SWAPNIL P. BADAR

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QUALIFICATION	• Bachelor of Engineering (Electronics & Telecomm) • Master of Technology (Electronics Engineering) • Doctorate of Philosophy (Pursuing)
AREA OF SPECIALIZATION	• VLSI Design
EXPERIENCE	• Teaching: 13 Years • Industrial: 1.5 Years
COURSES TAUGHT	• VLSI Design • CMOS Design • Network Analysis / Network Theory • Digital Electronics • Electronics Devices & Circuits • Electronics Devices & Components
MEMBERSHIP OF SCIENTIFIC AND PROFESSIONAL BODIES	• IEEE Graduate Student Member (Member ID- 97548153) –Annual- 2021-22. • IEEE Young Professionals • IEEE Robotics and Automation Society Membership • IEEE SIGHT
RESEARCH AND DEVELOPMENT	• To design and implement fast polar code decoder for 5G wireless application • 1024 bit Fast Simplified Successive Cancellation Polar Decoder is designed. • Simulation and synthesis is done using **Cadence Suite – Genus, Innovus, Virtuoso, Assura and Xilinx- ISE, Vivado**

PUBLICATIONS **Journals** **Conferences** **Books**	• S.P. Badar, K. B. Khanchandani, P. R. Wankhede**, "A Brief Study of Successive Cancellation Polar Decoder: Design and Performance Analysis,"** *SSGM Journal of Science and Engineering, Vol. 1 No. 1 (2023): Proceedings of INSCIRD-2023, pp.-146-150* • S. P. Badar, K. Khanchandani and P. Wankhede, **"Fast Polar Decoder Implementation using Special Nodes,"** *2023 2nd International Conference on Paradigm Shifts in Communications Embedded Systems, Machine Learning and Signal Processing (PCEMS)*, Nagpur, India, 2023, pp. 1-6, doi: 10.1109/PCEMS58491.2023.10136054. • S. P. Badar and K. Khanchandani, **"Successive Cancellation Polar Decoder Implementation using Processing Elements,"** *2022 IEEE Region 10 Symposium (TENSYMP)*, Mumbai, India, 2022, pp. 1-6, doi: 10.1109/TENSYMP54529.2022.9864529. • S. P. Badar and K. Khanchandani, **"Implementation of Combinational Logic for Polar Decoder,"** *2021 2nd International Conference on Range Technology (ICORT)*, Chandipur, Balasore, India, 2021, pp. 1-6, doi: 10.1109/ICORT52730.2021.9581844. • S. Badar and D. R. Dandekar, **"High speed FFT processor design using radix −4 pipelined architecture,"** *2015 International Conference on Industrial Instrumentation and Control (ICIC)*, Pune, India, 2015, pp. 1050-1055, doi: 10.1109/IIC.2015.7150901. • S. Badar and D. R. Dandekar, **"Review of Pipeline Architecture – Design Perspective,"** *in 3rd International Conference on Quality Up-gradation in Engineering, Science & Technology-2013 (IC-QUEST)* at BDCE, Sevagram on 19th April 2014.
FELLOWSHIP / AWARDS	• **Summer Faculty Research Fellowship at IIT Delhi** during 17th May 2023 to 08th July 2023. • Best Paper Award for the paper **"Implementation of Combinational Logic for Polar Decoder"** at 2nd IEEE International Conference on Range Technology (ICORT-2021) during 5th -6th August 2021. • **Certification** for **Training in Advanced Capabilities in Electronics Design and Manufacturing (TRIAC-EDM)** by NIELIT, India and III Taiwan- 2020-21.

	• **Summer Faculty Research Fellowship (Online) at IIT Delhi** during 1st June 2020 to 31st July 2020. • Secured 2nd rank for the project **"Design and Development of Analog Circuits using Unconventional CMOS Techniques for Biomedical Applications"** at National level Cadence Design Contest at Bangalore in Jan 2019.
Workshops/STTP/FDP Conducted as Resource Person	• Three Days Hands-on workshop on **"Basics of CMOS Design using Cadence"** at SSGMCE, Shegaon during 6th – 8th January and 24th - 26th March 2023. • Two Days Hands-on workshop on **"CMOS Digital Circuit Design"** at SSGMCE, Shegaon during 3rd – 4th December 2022. • Three Days Hands-on workshop on **"Verilog Hardware Description Language"** at SSGMCE, Shegaon during 4th – 6th March 2022. • One Week online workshop on **"CMOS Digital Circuit Design"** held at SSGMCE, Shegaon on 8th – 12th February 2021. • A Two Week Summer School on "**CMOS VLSI Circuit Design using Cadence"** held at SSGMCE, Shegaon during 17th – 29th June 2019. • Two Days Workshop on **"Hands on VLSI Circuit Design using Cadence"** held at SSGMCE, Shegaon on 2nd – 3rd March 2019 and 16th - 17th March 2019. • A Three Days Workshop on **"Hands on Digital VLSI Design using Xilinx"** held at SSGMCE, Shegaon during 8th - 10th September 2018 and 20th – 22nd September 2018. • A Four Week Summer School on "**CMOS VLSI Circuit Design using Cadence"** held at SSGMCE, Shegaon during 11th June – 7th July 2018. • A Two Days Workshop on **"Hands on VLSI Circuit Design using Cadence"** held at SSGMCE, Shegaon on 17th – 18th March 2018 and 31st March- 1st June 2018. • A Two Days Workshop on **"Hands on Digital System Design with Xilinx"** held at SSGMCE, Shegaon on 22nd – 23rd September 2017.
Workshops/STTP/FDP	• Four Days Workshop on **"MATLAB Based Apps Development"** held

Organized	on 30th July – 02nd August 2016 at SSGMCE, Shegaon. • One week Workshop on **"Industrial Automation"** during 10th – 16th September 2015 at SSGMCE, Shegaon. • Two Days Workshop on **"LATEX & its importance in Manuscript Preparation"** held on 18-19 March 2014 at BDCE, Sevagram. • Three Days Workshop on **"A Step towards Research with Networking Simulator (NS-2)"** held on 28th Feb-2nd March 2014 at BDCE, Sevagram. • Three days Workshop on **"Data Analysis Technique"** held on 16th - 17th August 2013 at BDCE, Sevagram. • Three days Workshop on **"VLSI Design using Tanner Tool"** held at BDCE, Sevagram during 7th - 9th March 2013
Workshops/STTP/FDP Attended/ Participated	• Participated & completed successfully Workshop on **"VLSI to System Design: Silicon to End use Application"** organized by Arm, STM and AICTE during 31st July to 4th August 2023. • Participated & completed successfully FDP on **"5G &B5G Wireless Technologies with MATLAB Practice"** , Supported by MEITY, Govt. of India organized by E&ICT Academy, PDPM IIITDM Jabalpur during 25th July – 5th August 2022. • Participated & completed successfully FTP on **"5G Wireless Communication Technology"** organized by IEEE India Council during 28th – 30th July 2022. • Participated & completed successfully SERB sponsored High End Workshop on **"Recent Trends in VLSI Devices, Circuits and Applications"** organized by ABV-IIITM, Gwalior. • Participated & completed successfully one week online FDP on **"Emerging Issues of VLSI Design"** organized by ITM University, Gwalior-MP-India during 6th - 10th September 2021. • Participated & completed successfully AICTE sponsored online STTP on **"Emerging Technologies of Opto-VLSI and Its Application"** organized by Meerut Institute of Engineering and Technology, Meerut

	31st August – 4th September 2021. • Participated in two days online workshop on **"Recent trends in FinFET & Nano-Sheet cell design"**- An educational perspective with 'Dr. Etienne Sicard' during 26th - 27th August 2021 organized by ni2design Pvt. Ltd., Pune. • Participated & completed successfully AICTE Training and Learning (ATAL) Academy Online FDP on **"ASIC Design for Driving Digital Innovations In Next Gen Platform Lab On Chip Engineering"** at AIT, Bangalore, Karnataka, India during 23rd - 27th August 2021. • Participated & completed successfully AICTE Training and Learning (ATAL) Academy Online FDP on **"VLSI -IP Design Approach to SRAM compiler design- Lab on Chip Engineering"** at GMIT, Davangere, Karnataka, India during 2nd - 6th August 2021. • Attended online FDP on **"Insights of NBA"** organized by the KCCEMSR, Thane during 28th - 30th June 2021. • Participated & completed successfully AICTE Training and Learning (ATAL) Academy Online FDP on **"IOT in 5G Technology"** at Silicon Institute of Technology, Bhubaneswar, Odisha, India during 5th – 9th May 2021. • Successfully completed online the AICTE-ISTE approved Orientation / Refresher Program **on "Advanced VLSI Design using Microwind"** organized by Dr. Rajendra Gode Institute of Technology & Research, Amravati, Maharashtra during 22nd – 28th April 2021. • Participated in a one week Faculty Development Program on **"Future Technologies for Smart Cities"** organized by SSGMCE, Shegaon during 1st – 5th February 2021. • Successfully completed the one week FDP – "**LeadScape Scholar-Warrior Program"** at SSGMCE, Shegaon during 27th Jan- 3rd Feb 2021. • Participated in a Two days online workshop on **"Internet of Things using Arduino through Tinkercad"** organized by TPAC, IEEE

	Bombay Section, IEEE Student's branch and Department of Electronics and Telecommunication Engg, SSGMCE, Shegaon during August 16th – 17th January 2021. • Participated in the online **"Summer Faculty Research Fellow Programme-2020"** under Continuing Education Program of Indian Institute of Technology (IIT) Delhi from 1st June to 31st July 2020 (Two months). • Successfully completed online Faculty Development Program on **"Electronic System Design, Modeling and Simulation"** organized by Pillai HOC College of Engineering and Technology, Rasayani during 8th – 10th June 2020. • Participated in Two Days Workshop on **"Creating a learning organization through outcome based measures"** organized by SSGMCE Shegaon , Maharashtra during June 11^{th} – 12^{th}, 2020 through online mode • Participated in Faculty Development Programme on **"Electronic System Design, Modeling and Simulation"** organized by Pillai HOC College of Engineering & Technology Rasayani , Maharashtra during June 8^{th} – 10^{th}, 2020 through online mode • Participated in Faculty Development Programme on **"Research Trends in VLSI Design"** held by NITTTR Chandigarh, during May 25^{th} – 29^{th}, 2020 through online mode. • Participated in Faculty Development Programme on **"Technological Inventions using wireless communication"** held by NITTTR Chandigarh, during May 18^{th} – 22^{th}, 2020 through online mode. • Participated in Five Days Workshop on **"Product Development"** organized by SSGMCE Shegaon , Maharashtra during April 13^{th} – 18^{th}, 2020 through online mode • Participated in Academy training programme on **"Specification to silicon: Advanced Analog CMOS IC Design"** held at MNIT, Jaipur, Rajasthan during November 3^{rd} – 5^{th}, 2017 under the aegis of E & ICT Academy sponsored by Ministry of Electronics & IT, Government of India.

	• Participated in Faculty Development Programme on **"Digital VLSI Circuit Design"** held at IIIT Jabalpur, Madhyapradesh during June 3rd – 12th, 2017 sponsored by Ministry of Electronics & IT, Government of India. • Participated in a Two-week ISTE STTP on **"CMOS, Mixed Signal & Radio Frequency VLSI Design "** conducted by IIT Kharagpur from 30th January – 4th February, 2017 held under the National Mission on Education through ICT(MHRD). • Attended a Course in **"Skill Development Program"** during 21st – 24th November 2016 at Mitsubishi Electric India Private Limited, Pune. • Attended a Three Days Workshop on **"Lab VIEW- basics and implementation for control, data acquisition & image processing"** during 23rd – 25th September 2016, jointly organized by CSIR-NCL, Pune and SSGMCE Shegaon. • Attended a Short Term Course on **"Wireless Technologies and Computer Architectures"** during 16th – 17th August 2016 at SSGMCE, Shegaon. • Participated in a three day Faculty Development Programme on **"PLC and Factory Automation"** during 19th – 21st June, 2016 held at SSGMCE, Shegaon sponsored by Mitsubishi Electric India Private Limited, Pune. • Participated in Three Days Workshop on **"Arduino using MATLAB"** organized by IEEE Students Branch, SSGMCE Shegaon during 28th – 30th December, 2015. • Attended a Two days workshop on **"Hands on Analog Design"** at Priyadarshni College of Engineering, Nagpur on 11th Jan-12th Jan 2013. • Attended One day workshop on **"Wireless Security"** at DMIETR, Salood (Wardha) on 13th April 2012. • Attended One week ISTE approved STTP on **Microcontrollers and Real World Interfacing** at BDCE, Sevagram on 14th June – 18th June 2010.